IN THE CLAIMS

Please amend the claims as follows:

1-3. (Cancelled)

4. (Currently amended) ~~The data latch timing adjustment apparatus of claim 1, including:~~ A data latch timing adjustment apparatus for adjusting latch timing of output data, the apparatus comprising:

a delay selecting section for delaying the output data with a plurality of delay amounts, generating a plurality of delayed output data pieces, and selecting and outputting one of the delayed output data pieces;

a latch circuit for receiving the delayed output data piece selected by the delay selecting section and a latch pulse signal, and latching the delayed output data piece at a time of receiving the latch pulse signal;

a delay control section for controlling the delay selecting section such that one of the delayed output data pieces with a delay amount different from that of the preceding delayed output data piece is selected by the delay selecting section and the current delayed output data piece is input to the latch circuit every time the latch pulse signal is input to the latch circuit;

a comparison circuit for comparing the data piece latched by the latch circuit with an associated checking data piece to determine whether or not the latched data piece and the checking data piece match each other; and

a determination section for receiving a plurality of comparison results from the comparison circuit, and determining, based on the comparison results, a delay amount in the delay selecting section with which the latch circuit latches the data piece appropriately.

5. (Currently amended) The data latch timing adjustment apparatus of claim 4, wherein [[if]] when the comparison results at the comparison circuit include successive matching results, the determination section determines that a delay amount located at the center of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

6. (Currently amended) The data latch timing adjustment apparatus of claim 4, wherein [[if]] when the comparison results at the comparison circuit include successive matching results, the determination section determines that the smallest one of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

7. (Currently amended) The data latch timing adjustment apparatus of claim 4, wherein [[if]] when the comparison results at the comparison circuit include successive matching results, the determination section determines that a delay amount shifted in consideration of a tendency in variation of an ambient temperature from a delay amount located at the center of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

8. (Original) The data latch timing adjustment apparatus of claim 4, wherein the determination section considers all the comparison results at the comparison circuit and determines that a delay amount in the delay selecting section associated with one of the comparison results having a high probability of being selected is an appropriate delay amount.

9-11. (Cancelled)

12. (Currently amended) ~~The data latch timing adjustment apparatus of claim 9, wherein~~

A data latch timing adjustment apparatus for adjusting latch timing of output data, the apparatus comprising:

a delay selecting section for delaying the output data with a plurality of delay amounts, generating a plurality of delayed output data pieces, and selecting and outputting one of the delayed output data pieces;

a latch circuit for receiving the delayed output data piece selected by the delay selecting section and a latch pulse signal, and latching the delayed output data piece at a time of receiving the latch pulse signal; and

a delay control section for controlling the delay selecting section such that one of the delayed output data pieces with a delay amount different from that of the preceding delayed output data piece is selected by the delay selecting section and the current delayed output data piece is input to the latch circuit every time the latch pulse signal is input to the latch circuit,

wherein the output data is data read out from a memory,

the latch circuit is provided in an LSI which receives the data read out from the memory,

the memory is a memory which outputs a strobe signal as well as the data, and

the latch pulse signal to be input to the delay selecting section is substituted by the strobe signal output from the memory.

13. (Original) The data latch timing adjustment apparatus of claim 4, wherein the output data is data of n (n is an integer of two or more) bits, and

the latch circuit and the comparison circuit are respectively provided n in number.

14. (Original) The data latch timing adjustment apparatus of claim 4, wherein the output data is data of n (n is an integer of two or more) bits,

the latch circuit is provided n in number,

the comparison circuit is provided singular in number, and

a selection section for selecting one of the n latch circuits is placed between the n latch circuits and the comparison circuit.

15. (Original) The data latch timing adjustment apparatus of claim 4, wherein the latch circuit latches the output data at rising and falling edges of the latch pulse signal, and

the delay selecting section, the latch circuit and the comparison circuit are provided in two sets such that one of the two sets is for a rising edge of the latch pulse signal and the other set is for a falling edge thereof.

16. (Original) The data latch timing adjustment apparatus of claim 15, wherein the output data is data read out from a memory which outputs a strobe signal as well as the data, and

the latch pulse signal is substituted by the strobe signal output from the memory.

17. (Currently amended) The data latch timing adjustment apparatus of claim 4, wherein the latch circuit latches the output data at rising and falling edges of the latch pulse signal,

the latch circuit and the comparison circuit are provided in two sets such that one of the two sets is for a rising edge of the latch pulse signal and the other set is for a falling edge thereof,

the delay selecting section is provided singular in number, and

the delayed output data piece selected by the delay selecting section [is] and a reverse signal of the delayed output data piece are input to the latch circuit for the rising edge and to the latch circuit for the falling edge, respectively.

18. (Original) The data latch timing adjustment apparatus of claim 17, wherein the latch pulse signal is input to the delay selecting section.

19. (Original) The data latch timing adjustment apparatus of claim 17, wherein the output data is input to the delay selecting section.

20. (Original) The data latch timing adjustment apparatus of claim 4, wherein the output data is data read out from a memory,

the checking data piece is stored in a checking data storing section beforehand, and

in reading the output data from the memory, the checking data piece stored in the checking data storing section is written into the memory prior to the readout of the output data, and then the checking data piece is read out as the output data from the memory.

21. (Original) The data latch timing adjustment apparatus of claim 20, wherein the checking data piece is stored in the checking data storing section in a pattern in which a crosstalk between adjacent bits in the memory is taken into consideration.

22. (Original) The data latch timing adjustment apparatus of claim 5, wherein after the determination section has determined the appropriate delay amount in the delay selecting section, the delay control section controls the delay selecting section such that delay amounts are sequentially increased or decreased relative to the appropriate delay amount in subsequent latch timing adjustments.

23. (Original) The data latch timing adjustment apparatus of claim 22, wherein in increasing or decreasing the delay amounts sequentially relative to the appropriate delay amount, the delay control section limits the increase or decrease of the delay amounts within a given range.

24. (Original) The data latch timing adjustment apparatus of claim 5, wherein the delay control section sequentially selects part of a plurality of delay amounts in the delay selecting section and determines that a range of delay amounts located among some of the part of the delay amounts with which the data piece is appropriately latched is a target of a next selection, and

in the next selection, the delay control section sequentially selects delay amounts included in the range of delay amounts which is the target of the selection to finally determine the appropriate delay amount based on one or more delay amounts with which the data piece is appropriately latched.

25. (New) A data latch timing adjustment apparatus for adjusting latch timing of output data, the apparatus comprising:

a delay selecting section for receiving a latch pulse signal, delaying the latch pulse signal with a plurality of delay amounts, generating a plurality of delayed latch pulse signals, and selecting and outputting one of the delayed latch pulse signals;

a latch circuit for receiving the output data and the delayed latch pulse signal selected by the delay selecting section, and latching the output data at a time of receiving the delayed latch pulse signal;

a delay control section for controlling the delay selecting section such that one of the delayed latch pulse signals with a delay amount different from that of the preceding delayed latch pulse signal is selected by the delay selecting section and the current delayed latch pulse signal is input to the latch circuit every time the delayed latch pulse signal is input to the latch circuit;

a comparison circuit for comparing the data piece latched by the latch circuit with an associated checking data piece to determine whether or not the latched data piece and the checking data piece match each other; and

a determination section for receiving a plurality of comparison results from the comparison circuit, and determining, based on the comparison results, a delay amount in the delay selecting section with which the latch circuit latches the data piece appropriately.

26. (New) The data latch timing adjustment apparatus of claim 25, wherein when the comparison results at the comparison circuit include successive matching results, the determination section determines that a delay amount located at the center of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

27. (New) The data latch timing adjustment apparatus of claim 25, wherein when the comparison results at the comparison circuit include successive matching results, the determination section determines that the smallest one of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

28. (New) The data latch timing adjustment apparatus of claim 25, wherein when the comparison results at the comparison circuit include successive matching results, the determination section determines that a delay amount shifted in consideration of a tendency in variation of an ambient temperature from a delay amount located at the center of a plurality of delay amounts in the delay selecting section associated with the successive matching results is an appropriate delay amount.

29. (New) The data latch timing adjustment apparatus of claim 25, wherein the determination section considers all the comparison results at the comparison circuit and determines that a delay amount in the delay selecting section associated with one of the comparison results having a high probability of being selected is an appropriate delay amount.

30. (New) A data latch timing adjustment apparatus for adjusting latch timing of output data, the apparatus comprising:

a delay selecting section for receiving a latch pulse signal, delaying the latch pulse signal

with a plurality of delay amounts, generating a plurality of delayed latch pulse signals, and selecting and outputting one of the delayed latch pulse signals;

a latch circuit for receiving the output data and the delayed latch pulse signal selected by the delay selecting section, and latching the output data at a time of receiving the delayed latch pulse signal; and

a delay control section for controlling the delay selecting section such that one of the delayed latch pulse signals with a delay amount different from that of the preceding delayed latch pulse signal is selected by the delay selecting section and the current delayed latch pulse signal is input to the latch circuit every time the delayed latch pulse signal is input to the latch circuit;

wherein the output data is data read out from a memory,

the latch circuit is provided in an LSI which receives the data read out from the memory,

the memory is a memory which outputs a strobe signal as well as the data, and

the latch pulse signal to be input to the delay selecting section is substituted by the strobe signal output from the memory.

31. (New) The data latch timing adjustment apparatus of claim 25, wherein the output data is data of n (n is an integer of two or more) bits, and

the latch circuit and the comparison circuit are respectively provided n in number.

32. (New) The data latch timing adjustment apparatus of claim 25, wherein the output data is data of n (n is an integer of two or more) bits,

the latch circuit is provided n in number,

the comparison circuit is provided singular in number, and

a selection section for selecting one of the n latch circuits is placed between the n latch circuits and the comparison circuit.

33. (New) The data latch timing adjustment apparatus of claim 25, wherein the latch circuit latches the output data at rising and falling edges of the delayed latch pulse signal selected by the delay selecting section, and

the delay selecting section, the latch circuit and the comparison circuit are provided in two sets such that one of the two sets is for a rising edge of the delayed latch pulse signal and the other set is for a falling edge of the delayed latch pulse signal.

34. (New) The data latch timing adjustment apparatus of claim 33, wherein the output data is data read out from a memory which outputs a strobe signal as well as the data, and

the latch pulse signal is substituted by the strobe signal output from the memory.

35. (New) The data latch timing adjustment apparatus of claim 25, wherein the latch circuit latches the output data at rising and falling edges of the delayed latch pulse signal selected by the delay selecting section,

the latch circuit and the comparison circuit are provided in two sets such that one of the two sets is for a rising edge of the delayed latch pulse signal and the other set is for a falling edge of the delayed latch pulse signal,

the delay selecting section is provided singular in number, and

the delayed latch pulse signal selected by the delay selecting section and a reverse signal of the delayed latch pulse signal are input to the latch circuit for the rising edge and to the latch circuit for the falling edge, respectively.

36. (New) The data latch timing adjustment apparatus of claim 35, wherein the latch pulse signal is input to the delay selecting section.

37. (New) The data latch timing adjustment apparatus of claim 35, wherein the output data is input to the delay selecting section.

38. (New) The data latch timing adjustment apparatus of claim 25, wherein the output data is data read out from a memory,

the checking data piece is stored in a checking data storing section beforehand, and

in reading the output data from the memory, the checking data piece stored in the checking data storing section is written into the memory prior to the readout of the output data, and then the checking data piece is read out as the output data from the memory.

39. (New) The data latch timing adjustment apparatus of claim 38, wherein the checking data piece is stored in the checking data storing section in a pattern in which a crosstalk between adjacent bits in the memory is taken into consideration.

40. (New) The data latch timing adjustment apparatus of claim 26, wherein after the determination section has determined the appropriate delay amount in the delay selecting section, the delay control section controls the delay selecting section such that delay amounts are sequentially increased or decreased relative to the appropriate delay amount in subsequent latch timing adjustments.

41. (New) The data latch timing adjustment apparatus of claim 40, wherein in increasing or decreasing the delay amounts sequentially relative to the appropriate delay amount, the delay control section limits the increase or decrease of the delay amounts within a given range.

42. (New) The data latch timing adjustment apparatus of claim 26, wherein the delay control section sequentially selects part of a plurality of delay amounts in the delay selecting section and determines that a range of delay amounts located among some of the part of the

delay amounts with which the data piece is appropriately latched is a target of a next selection, and

in the next selection, the delay control section sequentially selects delay amounts included in the range of delay amounts which is the target of the selection to finally determine the appropriate delay amount based on one or more delay amounts with which the data piece is appropriately latched.